8.5 A 65nm Low-Power Embedded DRAM with Extended Data-Retention Sleep Mode

Takeshi Nagai, Masaharu Wada, Hitoshi Iwai, Mariko Kaku, Atsushi Suzuki, Tomohisa Takai, Naoko Itoga, Takayuki Miyazaki, Hiroyuki Takenaka, Takehiko Hojo, Shinji Miyano

Toshiba, Kawasaki, Japan

Embedded DRAMs (eDRAMs) have superior features for mobile applications, notably low operation power and high bandwidth, compared with high-speed DRAMs such as DDR-SDRAM and XDR-DRAM. However, their standby power is not as attractive as their operation power because of the leakage of high-performance logic transistors and the fact that retention time of their memory cell is not as good as that of commodity DRAMs. For the purpose of reducing the standby power, lowering of BL swing in the refresh period has been reported [1]. However, this approach needs more frequent refresh operation due to a decrease in cell-charge. As a result, overall standby power is scarcely improved. To solve these problems, the extended data retention (EDR) sleep mode is introduced to a 65nm 32Mb eDRAM macro. The retention time is 8-times longer by ECC with no performance degradation.

By using ECC with the conventional redundancy, the tolerable number of random failure bits in the memory arrays is increased drastically. The inset in Fig. 8.5.1 shows the yield as a function of the average number of random single failure bits. Horizontal axis shows the ratio of the number of failure bits to the total number of memory cells in the 32Mb macro. Using the conventional redundancy, 0.00015% of average failure bits is tolerable without sacrificing yield. By using ECC, tolerable number of average failure bits increases to 0.015%. This enhancement of tolerance is very effective for extending the retention time of the worst cell after error correction. Figure 8.5.1 shows the typical retention-time distribution of the 65nm eDRAM. The retention time of the worst bit cell is extended by ECC to a length that is 8-times greater than in the case of only using the redundancy.

Figure 8.5.2 shows the concept of the EDR sleep mode. The timing diagrams of conventional macros are also shown for comparison. The refresh intervals with and without ECC, denoted by tREF and tREFECC, are shown in Fig 8.5.2 (a) and (b), respectively. In Fig. 8.5.2 (b), ECC is used in every read/write cycle and tREFECC is 8-times longer than tREF. However, the read/write speed deteriorates due to the check-bit generation and the error correction. To avoid these performance degradations, the EDR sleep mode shown in Fig. 8.5.2 (c) is proposed. The check bits are generated for all the cells at the beginning of the EDR sleep mode, and retention error bits failed in the sleep mode are corrected at the end of the EDR sleep mode. Since ECC operates only at the beginning and end of the sleep mode, the performance of read/write operation is not degraded. During the EDR sleep mode, the MT-CMOS technique with the leakage cut-off transistor is used to suppress the leakage current in the peripheral circuits because the period of refresh cycles is less than 0.1% of the tREFECC.

The block diagram of the 32Mb eDRAM macro is shown in Fig. 8.5.3 (a). The macro is divided into eight 4Mb sub-macros. Two groups of 136b global data lines are routed over the memory cell arrays. The 1b error within each 136b data-line group is corrected. The ECC circuits for check-bit generation and error detection are located on the lower side of the macro. The ECC control circuits are located at the center of the macro on the lower side. The block diagram of the ECC circuits is shown in Fig. 8.5.3 (b). In order to access all the cells in the macro, the addresses and the read/write command are generated in the ECC control circuit. At the beginning of the EDR sleep mode, the output data from the cells transferred through the RD bus are input to the check-bit generator and the generated check bits are written into the cells through the WD bus. At the end of the EDR sleep mode, all the data bits stored in the memory cells are read out again, and the read data is checked and corrected if errors are detected. The corrected data is written back to the memory cells through the WD bus.

Timing diagrams of the pipelined ECC operations are shown in Fig. 8.5.4. Figure 8.5.4 (a) shows the timing of the check-bit generation at the beginning of the sleep mode. Three clocks after each read command is issued, the read data from the memory cells come to the node Q. In the next cycle, the check bits are generated and then write command is issued. The generated check bits are written into the memory cells 4 cycles after the corresponding read command. By repeating the 4 consecutive read and the 4 consecutive write commands, waste cycles between read and write operation are eliminated.

At the end of the EDR sleep mode, this 4-read/4-write pipeline can be applied for the error correction. However, only few of the data need to be corrected during error correction, because the number of error bits is expected to be less than 0.05% of all of the memory cells. Here, the fast exit scheme is introduced in order to shorten the exit transition time. In this scheme, write-back operations are omitted when errors are not detected. Figure 8.5.4 (b) shows the timing of the error correction. The read commands are continuously issued until the ECC circuits detect error in data. When an error is detected, a write command is issued and the corrected data is written into the memory cells of the corresponding address. Since more than 99.5% of data do not need to be written, the period for exiting sleep mode becomes almost half compared with the 4-read/4-write operation, as shown in Fig. 8.5.5 (a).

Figure 8.5.5 (b) shows the block diagrams of the address and command controller. The fail address register keeps the prior 4 cycle addresses. When an error is found in the read data, the DETECTp from the error-detect circuits in Fig. 8.5.3 (b) becomes high and the WRITE command is issued at the next cycle. The corresponding column address for this WRITE command comes from the fail address register.

Figure 8.5.6 shows a comparison of the estimated data-retention power of the 32Mb eDRAM macro between normal mode and the EDR sleep mode. In the normal mode, 1480μW of the refresh power and 1590μW of the leakage power are consumed as the standby power. In the EDR sleep mode, the refresh power is reduced to 1/8, and the leakage power is reduced to 208μW by the MT-CMOS technique. The total data-retention power of the 32Mb macro at 85°C is reduced from 3.07mW to 393μW by using the EDR sleep mode.

A 65nm 300MHz 32Mb eDRAM macro with the EDR sleep mode is presented for the mobile application. Figure 8.5.7 shows the chip micrograph of the eDRAM macro with the detailed features of the design. The data-retention power is reduced with no performance penalty by the proposed EDR sleep-mode architecture in this eDRAM macro. Consequently, the simulation results show that the page-mode operation of 400MHz is realized.

Acknowledgements:
The authors would like to thank the members of the embedded memory design team for their support. They are also grateful to Y. Watanabe for his support and encouragement.

Reference:
[1] F. Morishita, et al., "A 312MHz 16Mb Random-Cycle Embedded DRAM Macro with 73μW Power-Down Mode for Mobile Applications," *ISSCC Dig. Tech. Papers*, pp. 202-203, Feb., 2004.

 1-4244-0079-1/06/$20.00

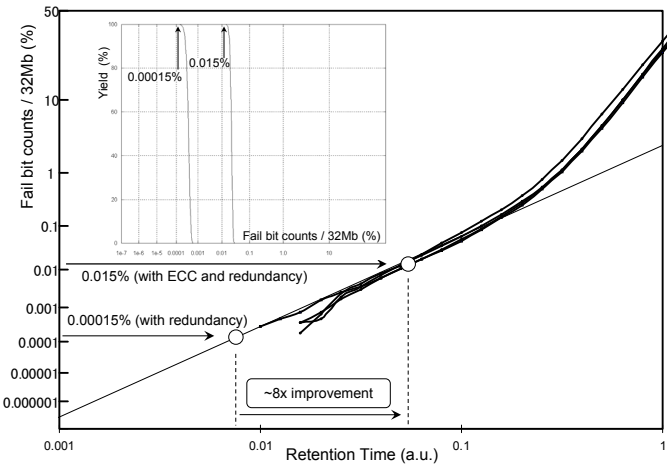


Figure 8.5.1: Retention time distribution.

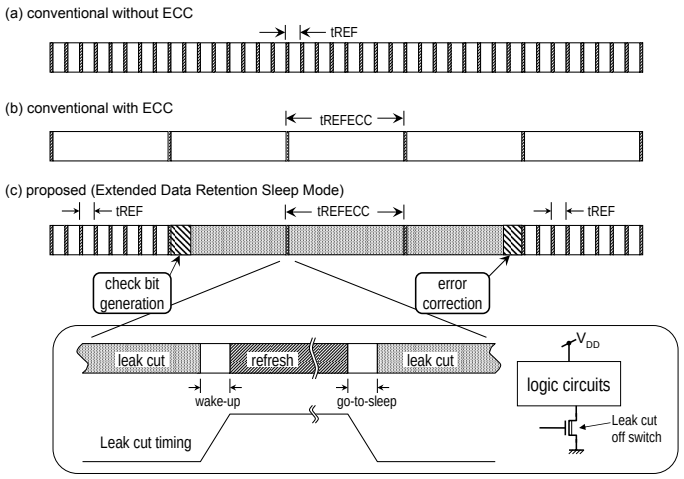


Figure 8.5.2: Concept of the extended data-retention sleep mode.

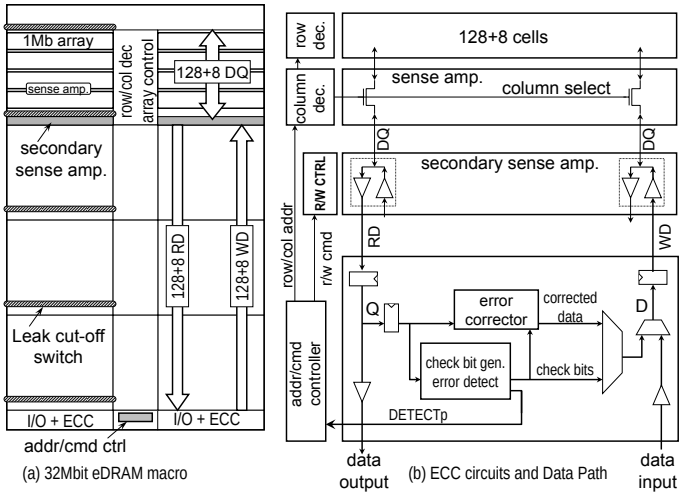


Figure 8.5.3: Block diagram of the eDRAM macro.

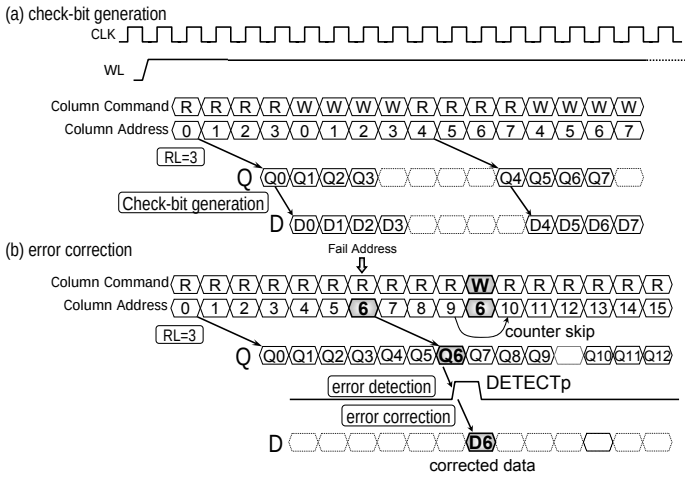


Figure 8.5.4: Timing diagram of the pipelined ECC operations.

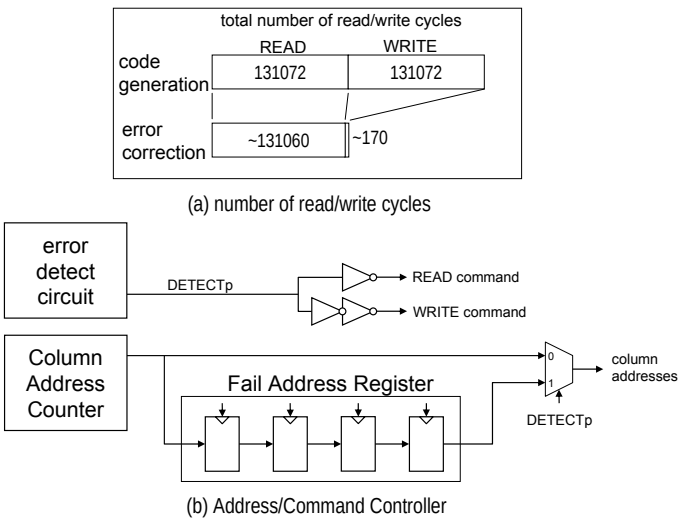


Figure 8.5.5: Block diagram of Address/Command Controller.

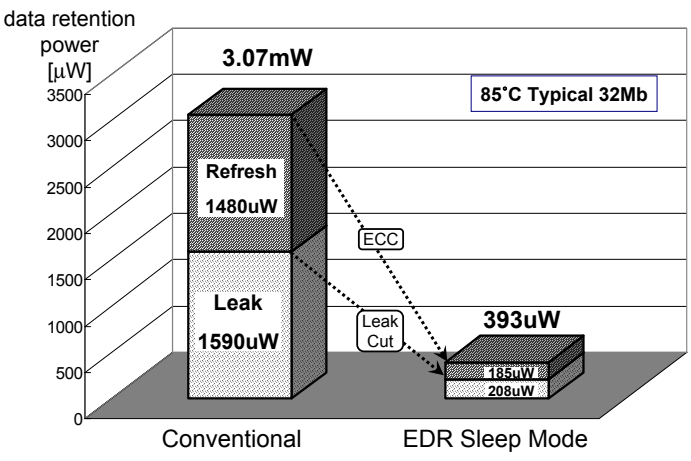
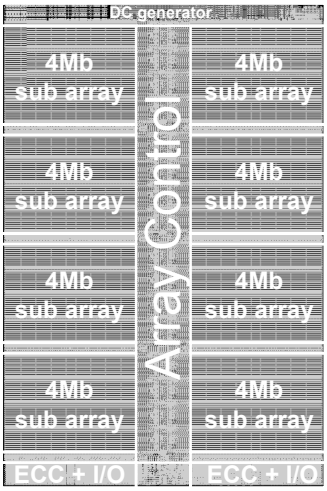


Figure 8.5.6: Estimated data-retention power.

Continued on Page 645



Technology	65nm 5 layer metal (Cu)
Dual Tox	1.8nm/7.0nm
Cell Size	0.20 x 0.55um^2
Power Supply (V)	V_{DD}=1.2V, V_{PP}=3.3V
I/O	128/256
#Banks	1,2,4
Command I/F	SDRAM
Macro Size	2190 x 3580μm^2
Data Retention Power	0.39mW@ 85˚C

Figure 8.5.7: Chip micrograph and its features.

